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## SEMICONDUCTOR DEVICE

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### CROSS-REFERENCE TO RELATED APPLICATION

This application claims priority from copending application serial number 60/490,239 filed on July 25, 2003, which is hereby incorporated by reference herein.

### BACKGROUND

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Thin-film transistors and other three-port semiconductor devices typically include three electrodes separated in part by a channel material. In many such devices, one of the electrodes is further separated from the other electrodes by a dielectric material, as is the case with the gate electrode in a thin-film transistor. In a thin-film transistor, and in other transistors having a gate electrode, the voltage applied to the gate electrode controls the behavior of the channel material. Specifically, the applied gate voltage controls the ability of the channel material to permit charge transport through the channel material between the other two electrodes (e.g., a source electrode and drain electrode).

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Extensive research has been conducted with respect to the materials used to fabricate the different components in thin-film transistors. Though materials that have been used for thin film transistors may be suitable for many applications, it will in some cases be desirable to have channel layers formed from other materials. Other materials may provide certain performance or processing benefits, result in cost savings and/or provide characteristics that are difficult to achieve otherwise.

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### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 depicts an embodiment of an exemplary three-port semiconductor device according to the present description, in the form of a thin-film transistor.

Fig. 2 depicts an embodiment of an exemplary dielectric layer that may be implemented in connection with the three-port semiconductor device of Fig. 1.

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Fig. 3 depicts an embodiment of an exemplary display system in which the semiconductor devices of the present description may be employed.

Fig. 4 depicts an exemplary method of using the three-port semiconductor devices of the present description.

5 Figs. 5-8 depict further exemplary embodiments of a thin-film transistor according to the present description.

#### DETAILED DESCRIPTION

The present description pertains to a system and method involving a multi-port semiconductor device in which a novel configuration is employed in one or  
10 more of the charge-carrying portions of the device. The present system and method is applicable to a variety of semiconductor applications, but has proved particularly useful in the context of thin-film transistor (TFT) technologies, and more particularly in TFTs that are at least partially transparent.

Fig. 1 depicts an exemplary three-port semiconductor device according to  
15 the present description, such as thin-film transistor (TFT) 10. As shown, TFT 10 may employ a bottom-gate structure, in which material comprising a gate electrode 12 is disposed adjacent a substrate 14. A dielectric 16 is disposed atop gate 12. A channel layer 18 is interposed between dielectric 16 and source electrode 20 and drain electrode 22. Electrical conditions existing at gate  
20 electrode 12 (e.g., a gate voltage applied to port 24) determine the ability of the device to transport charge through channel 18 between source 20 and drain 22 (e.g., as current flowing through the channel between ports 26 and 28).

It will be appreciated that a variety of different fabrication techniques and materials may be employed to fabricate a thin-film transistor, such as that shown  
25 in the figure. In the depicted example, substrate 14 may be formed from glass and coated with a material such as indium-tin oxide (ITO) to form the gate electrode. Although the gate electrode and dielectric are depicted as blanket-coated, unpatterned layers in Fig. 1, they may in general be patterned as appropriate. A channel layer is disposed over the dielectric, as will be explained,  
30 and indium-tin oxide contacts are disposed for the source and drain electrodes. Regardless of the particular fabrication techniques, the different regions are disposed/configured so that: the source and drain electrodes are physically

separate from one another (e.g., separated by the channel material); the three ports (source, drain and gate) are physically separated from each other (e.g., by the dielectric and channel); and the dielectric separates the gate from the channel. Also, as discussed below and shown in the depicted examples, the source and drain are coupled together by the channel.

In addition, the dielectric layer (e.g., dielectric 16) may be formed with alternating layers of different materials, such as  $\text{AlO}_x$  and  $\text{TiO}_y$  layers. In particular, as shown in Fig. 2, dielectric layer 16 may include interior layers of type A and type B, where type A is formed from  $\text{AlO}_x$  and type B is formed from  $\text{TiO}_y$  (x and y being positive nonzero values), or vice versa. The outer layers (designated with C) may be formed from or coated with a cap layer of  $\text{Al}_2\text{O}_3$  or another suitable material. Specifically, the dielectric sub-layer immediately adjacent and in contact with gate electrode 12 may be  $\text{Al}_2\text{O}_3$  and the layer immediately adjacent and in contact with channel 18 may be  $\text{Al}_2\text{O}_3$ .

The ITO source/drain contacts may be deposited via ion beam sputtering, in the presence of argon and oxygen, or through other suitable deposition methods. The source and drain contacts may be disposed via patterning with shadow masks or the like, or through other suitable patterning methods.

As indicated in Figs. 1 and 4 (Fig. 4 depicts a method to be explained below), channel 18 may be fabricated employing a ternary material containing zinc, tin and oxygen. These more complicated materials (e.g., ternary compounds and materials having more than three elemental components) tend to be less predictable, and often have structures that are much less ordered than binary compounds. Indeed, ternary compounds are often amorphous. Less ordered materials (e.g., amorphous materials) are typically dramatically less efficient at permitting charge transport. For example, amorphous silicon is a very poor semiconductor material, relative to crystalline silicon.

Accordingly, experimental results revealing a high degree of charge mobility in the present ternary channel material were unexpected. Even more unexpected were findings showing adequate charge mobility in certain amorphous zinc-tin oxides.

A variety of zinc-tin oxide materials may be employed within the channel 18 to provide suitable performance in a thin film transistor. Particular formations that have proven useful include  $\text{ZnSnO}_3$ ,  $\text{Zn}_2\text{SnO}_4$ , and/or combinations thereof. More generally, zinc-tin oxide materials of interest herein may comprise the  
5 compositional range  $(\text{ZnO})_x(\text{SnO}_2)_{1-x}$ , with  $x$  between 0.05 and 0.95. While the formulations listed above refer only to stoichiometry (i.e., the relative quantities of zinc, tin, and oxygen in a given zinc-tin oxide material), a variety of morphologies may be obtained depending on composition, processing conditions, and other factors. For example, a zinc-tin oxide film may be either substantially amorphous  
10 or substantially poly-crystalline; a poly-crystalline film may furthermore contain a single crystalline phase (e.g.,  $\text{Zn}_2\text{SnO}_4$ ) or may be phase-segregated so that the channel contains multiple phases (e.g.,  $\text{Zn}_2\text{SnO}_4$ ,  $\text{ZnO}$ , and  $\text{SnO}_2$ ). The channel layer 18 may be disposed adjacent dielectric layer 16, through various methods. In the depicted example, the channel is disposed using RF sputtering in an  
15 argon-oxygen atmosphere, and patterned using shadow masks.

The zinc-tin oxide semiconductor devices of the present disclosure may be employed in a variety of different applications. One application includes deployment of the zinc-tin oxide channel within thin-film transistors used in an active matrix display, such as that shown at 40 in Fig. 3. In display applications  
20 and other applications, since zinc-tin oxide is itself transparent, it will often be desirable to fabricate one or more of the remaining device layers (i.e., source, drain, and gate electrodes) to be at least partially transparent.

Referring still to Fig. 3, Exemplary display 40 includes a plurality of display elements, such as pixels 42, which collectively operate to display image data.  
25 Each pixel may include one or more thin-film transistors, such as that described above with reference to Figs. 1 and 2, in order to selectively control activation of the pixels. For example, each pixel may include three thin-film transistors, one for each of a red, blue and green sub-pixel. In such a display, device 10 (Fig. 1) may be employed as a switch to selectively control activation of the sub-pixel.  
30 For example, application of a turn-on voltage at the gate (e.g., applying a HI voltage to gate port 24) may enable current to flow through channel 18 and

thereby activate a light-emitting or light-controlling element of the desired hue (e.g., red, green, blue, etc.).

Fig. 4 depicts an example of such a switching method, as may be employed in connection with an active matrix display, or in other settings requiring switching. At 60, the method includes providing a semiconductor device having a channel region formed from compound having zinc, tin and oxygen. At 62, the semiconductor device is coupled into a switching configuration. Referring to the display example, discussed above with respect to Fig. 3, this may include configuring the semiconductor device as a current source switch that controls whether current is applied to a light-emitting display element. In addition, the device may control how much current is supplied, instead of simply acting in a binary mode as an on-off switch. At 64, Fig. 4 depicts an example of the specific control mechanism, namely, that the state of the switch may be controlled in response to a gate voltage. Referring to Fig. 1, such a controlling gate voltage may be applied at port 24 to enable channel 18, and thereby increase the ability of channel 18 to permit charge transport in response to electric potential applied across terminals 26 and 28.

It will be appreciated that various different transistor configurations may be employed in connection with the thin-film devices of the present disclosure. Further exemplary thin-film transistor configurations are shown in Figs. 5-8. From this and the prior examples, it will be appreciated that typical configurations will include: (a) three primary electrodes, designated in the examples of Figs. 5-8 as the gate 80, source 82 and drain 84; (b) a dielectric material 90 interposed between gate electrode 80 and each of the source and drain electrodes 82 and 84, such that dielectric material 90 physically separates the gate from the source and drain; (c) a semiconductive material, referred to as the channel 92, disposed so as to provide a controllable electric pathway between the source electrode and the drain electrode. In such a configuration, as known in the transistor arts and discussed with reference to the examples discussed above, voltage applied at gate electrode 80 varies the ability of channel 92 to permit electrical charge to move between the source and drain electrodes. The conductive properties of the

channel are thus controlled at least in part through application of a voltage at the gate electrode.

Channel 92 (and the channel of the previous examples) typically is deposited as a thin layer immediately adjacent the dielectric material. Indeed, it will be appreciated that the depictions in the figures are exemplary and are intended to be schematic. The relative dimensions of a device constructed according to the present description, or of its constituent parts, may vary considerably from the relative dimensions shown in the present figures.

Still referring to Figs. 5-8, regardless of the sequence in which channel 92 and source/drain electrodes 82 and 84 are deposited and patterned, the resulting configuration typically is as described above, namely that the channel is positioned so as to provide a controllable charge pathway between the source and drain electrodes, and dielectric 90 physically separates the channel and gate electrode 80. As previously discussed, it will often be desirable to fabricate the channel from a zinc-tin oxide material.

As in the depicted examples, a thin-film transistor according to the present description may take a variety of different configurations. Figs. 5 and 6 show exemplary thin-film transistors having a bottom gate configuration. A substrate 100 is employed, though configurations omitting a substrate are possible. Gate electrode 80 is then deposited and patterned as appropriate. Dielectric 90 is deposited on top of the gate electrode and is patterned as appropriate. The channel 92 and source and drain electrodes 82 and 84 are then deposited and patterned as appropriate. In the example of Fig. 5, the source and drain electrodes are formed first, and then channel 92 is deposited on top of the source and drain electrodes. In the example of Fig. 4, channel 92 is deposited first, and the source/drain electrodes are subsequently deposited.

A top gate structure may be employed, as in the examples of Figs. 7 and 8. In such a configuration, a substrate 100 may again be employed, but the source 82, drain 84 and channel 92 are formed prior to depositing of the layers comprising dielectric 90 and gate electrode 80. In the example of Fig. 7, channel 92 is deposited first as a thin film, and source 82 and drain 84 are deposited and patterned on top of the deposited channel layer. In the example of Fig. 8,

channel 92 is deposited on top of the already-formed source and drain electrodes 82 and 84. In either case, dielectric 90 is deposited next and patterned as appropriate, and gate electrode 80 is deposited and patterned on top of dielectric 90.

5           While the present embodiments and method implementations have been particularly shown and described, those skilled in the art will understand that many variations may be made therein without departing from the spirit and scope defined in the following claims. The description should be understood to include all novel and non-obvious combinations of elements described herein, and claims  
10   may be presented in this or a later application to any novel and non-obvious combination of these elements. Where the claims recite "a" or "a first" element or the equivalent thereof, such claims should be understood to include incorporation of one or more such elements, neither requiring nor excluding two or more such  
15   elements.